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|---|-------------|----------------------|---------------------|------------------|
| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
| 10/810,094 | 03/26/2004 | Mark D. Matson | BP3197 | 8200 |
| 51472 | 7590 | 03/27/2009 | | |
| GARLICK HARRISON & MARKISON P.O. BOX 160727 AUSTIN, TX 78716-0727 | | | EXAMINER | |
| | | | WENDELL, ANDREW | |
| ART UNIT | | PAPER NUMBER | | |
| 2618 | | | | |
| MAIL DATE | | DELIVERY MODE | | |
| 03/27/2009 | | PAPER | | |

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARK D. MATSON and BRUCE E. EDWARDS

Appeal 2009-0213
Application 10/810,094
Technology Center 2600

Decided:¹ March 27, 2009

Before KENNETH W. HAIRSTON, ROBERT E. NAPPI,
and CARLA M. KRIVAK, *Administrative Patent Judges*.

KRIVAK, *Administrative Patent Judge*.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134 from a final rejection of claims 1-20. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

¹ The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF CASE

Appellants' claimed invention is a method and system for reducing power consumption in a communication system (Spec. 1: ¶[001]). More particularly, Appellants' invention provides an improved method and system for controlling the sleep and wake-up modes of a processor (Spec. 3: ¶[008]). The processor and associated modules are quickly powered down and efficiently reactivated by powering up only the processor and the required modules necessary to respond to the asserted wake-up conditions (Spec. 4: ¶[008]).

Independent claim 1, reproduced below, is representative of the subject matter on appeal.

1. A data processor for use in a wireless communication, comprising:
 - a processing unit;
 - an instruction pipeline circuit;
 - at least one processing module;
 - a timer for generating a time-out interval; andpower control logic for detecting a sleep instruction and placing the processing unit, instruction pipeline circuit and at least one processing module in a low-power state, where the power control logic is operative in response to a wake-up signal to reactivate the instruction pipeline circuit, and consequently at least one processing module only to the extent required by the wake-up signal.

REFERENCES

| | | |
|----------|-------------------|---------------|
| Karoaguz | US 2002/005934 A1 | May 16, 2002 |
| Shohara | US 6,473,607 B1 | Oct. 29, 2002 |

| | | |
|----------|--------------------|---------------|
| Fukuhara | US 2003/0028677 A1 | Feb. 6, 2003 |
| Lindskog | US 6,622,251 B1 | Sep. 16, 2003 |

The Examiner rejected claims 11-18 under 35 U.S.C. § 101.

The Examiner rejected claims 1, 2, 4-6, 8, 10, 11, and 13-18 under 35 U.S.C. § 102(b) based upon the teachings of Shohara.²

The Examiner rejected claim 3 under 35 U.S.C. § 103(a) based upon the teachings of Shohara and Fukuhara.

The Examiner rejected claims 7, 12, 19, and 20 under 35 U.S.C. § 103(a) based upon the teachings of Shohara and Lindskog.

The Examiner rejected claims 9 and 15 under 35 U.S.C. § 103(a) based upon the teachings of Shohara and Karaoguz.

Appellants contend that, with respect to the rejection under 35 U.S.C. § 101, the Amendment filed September 6, 2007, to claim 11 should be entered as it was made in compliance with the Examiner's requirement (Br. 5). The Appellants also contend that Shohara fails to disclose an "instruction pipeline circuit" much less "using detected sleep instructions and wakeup signals to selectively power down and reactivate processing modules in the instruction pipeline circuit only to the extent required by the sleep instruction and the wake-up signal" (Br. 5).

ISSUES

Did the Examiner err in finding claims 11-18 do not meet the requirements of 35 U.S.C. § 101?

² It appears the Examiner inadvertently did not include claim 8 in the rejection on page 4 of the Answer, however, the Examiner addressed claim 8 on page 5 of the Answer.

Did the Examiner err in finding the “instruction pipeline circuit” in claims 1, 2, 4-6, 8, 10, 11, and 13-18 is anticipated by Shohara under 35 U.S.C. § 102(b)?

Did the Examiner err in finding claims 3, 7, 9, 12, 15, 19 and 20 obvious over the teachings of Shohara, Lindskog, Karaoguz?

FINDINGS OF FACT

1. Appellants’ invention provides effective power savings by deactivating all instruction pipeline stages (instruction fetch, instruction decode, etc.) and other external modules, and then selectively reactivating only the modules needed to service the wake-up condition (Spec. 14: ¶¶[039], [040]).

2. Shohara teaches a self-calibrating sleep timer. A controller scheduling means schedules commands for supervision of a communication device, particularly as it relates to power savings, by writing command records to an event scheduler (col. 5, ll. 29-32). The event scheduler “provides registers for records of scheduled events...comprising a command word that initiates a processing event and the scheduled system time for execution of said command” (col. 6, ll. 59-62). The scheduled commands include commands to the power controller to “selectively power up or power down components of the communication device at specified event times” (col. 7, ll. 1-3); commands to “switch the state from sleep mode to active mode at specified event times” (col. 7, ll. 4-7); commands to “generate interrupts to execute controller algorithms and operations” (col. 7, ll. 8-13; and commands for “receiver downconversion and demodulation of a scheduled message” (col. 7, ll. 14-15).

3. Shohara further teaches that the power controller provides switching of power, typically from a battery, “to the components of the communication device on a need basis so that only essential components are powered on at any time” (col. 12, ll. 57-61). The power controller is responsive to switching commands from the controller or a timer (col. 6, ll. 61-64).

4. An instruction pipeline is used in the design of computers and other digital electronic devices for increasing instruction throughput. Pipeline instruction execution is an implementation technique where multiple instructions are overlapped in execution.³

PRINCIPLES OF LAW

Descriptive material can be characterized as either “functional” or “non-functional.” *Manual of Patent Examining Procedure* (MPEP) § 2106.01 (Eighth Ed., Rev. 6, Sept. 2007).⁴ Reciting either type of descriptive material per se, however, is nonstatutory. *See In re Warmerdam*, 33 F.3d 1354, 1360-61 (Fed. Cir. 1994); *see also* MPEP § 2106.01 (discussing functional and non-functional descriptive material when claimed as descriptive material per se). Further, “[w]hen nonfunctional descriptive

³ See Processor Architecture, Jurij Šilc, et al., particularly Glossary, p. 354.

⁴ “Non-functional” descriptive material, such as music, literary works, and compilations or mere arrangements of data, lacks any functional interrelationship and therefore does not fall into any of the enumerated statutory categories. *Manual of Patent Examining Procedure*, § 2106.01, Rev. 6, Sept. 2007. “Functional” descriptive material, on the other hand, has been characterized in the computer context as consisting of data structures and programs that impart functionality when employed as a computer component. *Id.*

material is recorded on some computer-readable medium, in a computer or on an electromagnetic carrier signal, it is not statutory since no requisite functionality is present to satisfy the practical application requirement.” MPEP, *id.*

“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros., Inc. v. Union Oil Co. of Calif.*, 814 F.2d 628, 631 (Fed. Cir. 1987).

During examination of a patent application, a claim is given its broadest reasonable construction “in light of the specification as it would be interpreted by one of ordinary skill in the art.” *In re Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004).

ANALYSIS

§101 Non-Statutory Subject Matter

The Examiner rejected claims 11-18 under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter. The Examiner finds that claims 11-18 are “drawn to a ‘program’ per se as recited in the preamble and as such is non-statutory subject matter” (Ans. 3). The Examiner further finds that amending the claim to recite “‘computer readable medium encoded with a computer program’ would make the claim statutory” (Ans. 4).

Claim 11 recites “[a]n article of manufacture having at least one recordable medium having stored thereon executable instructions and data which, when executed by at least one processing device, cause the at least one processing device to...” Thus, claim 11 includes a recordable medium

having stored executable instructions and data to cause the processing device to carry out specific functions such as detecting a sleep instruction, specifying wake-up and time-out intervals, reactivating the instruction pipeline, etc. Accordingly, the Examiner is not correct that claims 11-18 are drawn to a “program” per se since claim 11 is capable of causing functional change. Thus, requisite functionality is present to satisfy the practical application requirement of §101. Amending the preamble to recite a “computer readable memory encoded with a computer program” would be similar to the language already used: “at least one recordable medium having stored thereon executable instructions and data...” Therefore, claim 11 along with claims 12-18, which depend therefrom, are directed to statutory subject matter and meet the requirements of 35 U.S.C. § 101.

Anticipation Under 35 U.S.C. § 102(b)

The Examiner rejected claims 1, 2, 4-6, 8, 10, 11, and 13-18 under 35 U.S.C. § 102(b) as anticipated by Shohara. The Examiner finds that all the claim limitations read on Shohara (Ans. 4-5). This rejection is addressed with respect to claim 1, as independent claim 11 includes substantially the same features Appellants addressed, and Appellants argued these claims together (Br. 5).⁵

Appellants contend that Shohara fails to disclose the “instruction pipeline circuit” (Br. 5). Appellants further contend that the Examiner’s assertion that “any circuit that carries out instructions (i.e. control

⁵ The Supplemental Appeal Brief filed February 29, 2008, in addition to the Appeal Brief filed January 29, 2008, is what are referred to throughout this Opinion as the Brief (Br.).

information) to other components through channels (i.e. connections) can be considered an instruction pipeline given the broadest responsible (sic. reasonable) interpretation" (Br. 5; Final Office Action 9; Ans. 10-11).

Although the Examiner is correct that a broad interpretation of a pipe line would include a circuit that carries instructions to other components through channels, the Examiner has not considered that the term "instruction pipeline circuit" is a term of art having a particular meaning as shown by Appellants' evidence (Appendix D). That is, an instruction pipeline is used in the design of computers and other digital electronic devices for increasing instruction throughput. Pipeline instruction execution is an implementation technique where multiple instructions are overlapped in execution (FF 4). Shohara does not teach pipelining or an instruction pipeline circuit (FF 2, 3).

Because Shohara does not teach an instruction pipeline circuit as known in the art (FF 4) and addressed in the specification, independent claims 1 and 11 do not read on Shohara. Thus, Shohara does not anticipate independent claims 1 and 11, or dependent claims 2, 4-6, 8, 10, and 13-18.

Obviousness

The Examiner rejected claims 3, 7, 9, 12, 15, 19, and 20 as obvious under 35 U.S.C. § 103 over various combinations of Shohara, Fukuhara, Lindskog, and Karaoguz. Claims 3, 7, and 9 depend from claim 1 and claims 12 and 15 depend from claim 11. These claims are addressed with respect to representative claim 1.

Shohara does not teach or suggest the pipeline circuit, as set forth above, and Fukuhara, Lindskog, and Karaoguz do not cure the deficiencies of Shohara (App. Br. 8). Claims 3, 7, 9, 12, 15, and 20, include the pipeline

circuit and thus, are not obvious over the collective teachings of these references.

Claim 19 was rejected as being obvious over Shohara and Lindskog (Ans. 7, 8). Claim 19 includes substantially the same limitations recited in claims 1 and 11, except it does not recite an instruction pipeline.

Appellants' arguments are directed only to the instruction pipeline (App. Br. 8). These arguments are not commensurate in scope with the limitations in claim 19. As set forth above, Shohara teaches all the limitation of claim 19. Appellants have provided no convincing arguments that the Examiner erred in finding that the teachings of Shohara and Lindskog suggest Appellants' invention. Thus, claim 19 is obvious over the collective teachings of Shohara and Lindskog.

CONCLUSION

The Examiner erred in rejecting claims 11-18 under 35 U.S.C. § 101.

The Examiner erred in rejecting claims 1, 2, 4-6, 8, 10, 11, and 13-18 under 35 U.S.C. § 102.

The Examiner erred in rejecting claims 3, 7, 9, 12, 15, and 20 under 35 U.S.C. § 103.

The Examiner did not err in rejecting claim 19 under 35 U.S.C. § 103.

DECISION

The Examiner's decision rejecting claims 1-18 and 20 is reversed.
The Examiner's decision in rejecting claim 19 is affirmed.

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Application 10/810,094

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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